In the Claims:

Pursuant to 37 C.F.R. § 1.121(c) and the revised amendment practice effective July 30, 2003, please amend claims 6-8 as indicated herein. A complete listing of all the claims in the application is provided immediately below.

COMPLETE LISTING OF ALL CLAIMS IN THE APPLICATION

1. (original) A frequency-sensitive electrical circuit, comprising:

first and second inputs;

at least one transformer circuit having a first winding connected to the first input and a second winding connected to the second input;

a first load connected in parallel to the first winding;

a second load connected in parallel to the second winding;

first and second outputs connected to the first and second windings, respectively; and

a capacitor connected between the first and second outputs.

2. (original) The circuit of claim 1, wherein a signal carrying both voice and data information is received at the first and second inputs.

3. (original) The circuit of claim 1, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs.

4. (original) The circuit of claim 1, wherein the circuit reduces the distortion of a signal received at the first and second inputs and delivered at the first and second outputs.

5. (original) The circuit of claim 1, further comprising a third output, connected via a second capacitor to the first input, and a fourth output, connected via a third capacitor to the second input.

6. (currently amended) A frequency-sensitive electrical circuit, comprising:

a first stage having first and second inputs and first and second outputs, the first stage comprising

a parallel-connected first inductor and first resistor, connected between the first input and first output,

a parallel-connected second inductor and second resistor, connected between the second input and second output, the first and second inductors being inductively coupled, and

a first capacitor connected between the first and second outputs.

7. (currently amended) The circuit of claim 6, further comprising:

a second stage having first and second inputs and first and second outputs, the ~~first~~ second stage comprising

a parallel-connected ~~first~~ third inductor and ~~first~~ second capacitor, connected between the first input and first output of the second stage,

a parallel-connected ~~second~~ fourth inductor and ~~second~~ third capacitor, connected between the second input and second output of the second stage, the ~~first~~ third and ~~second~~ fourth inductors being inductively coupled, and

a ~~third~~ fourth capacitor connected between the first and second outputs of the second stage,

wherein the first and second outputs of the second stage ~~are operatively connected to~~ form the first and second inputs of the first stage, respectively.

8. (currently amended) The circuit of claim 6, further comprising:

a ~~third~~ second stage having first and second inputs and first and second outputs, the ~~first~~ second stage comprising

a ~~first~~ third inductor connected between the first input and first output of the second stage,

a ~~second~~ fourth inductor connected between the second input and second output of the second stage, the ~~first~~ and second inductors being inductively coupled, and

amplifying element.

a second capacitor connected between the first and second outputs of the second stage,

wherein the first and second outputs of the ~~third~~ second stage ~~are operatively connected to~~ form the first and second inputs of the first stage, respectively.

9. (original) The circuit of claim 6, wherein a signal carrying both voice and data information is received at the first and second inputs.

10. (original) The circuit of claim 6, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs.

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11. (original) The circuit of claim 6, wherein the circuit reduces the distortion of a signal received at the first and second inputs and delivered at the first and second outputs.

12. (original) The circuit of claim 6, further comprising a third output, connected via a second capacitor to the first input, and a fourth output, connected via a third capacitor to the second input.

13. (original) A telecommunications signal splitter, comprising:

first and second signal inputs;

at least one transformer circuit having a first winding connected to the first signal input and a second winding connected to the second signal input;

a first load connected in parallel to the first winding;

a second load connected in parallel to the second winding;

first and second outputs connected to the first and second windings, respectively; and

a capacitor connected between the first and second outputs.

14. (original) The circuit of claim 13, wherein a signal carrying both voice and data information is received at the first and second inputs.

15. (original) The circuit of claim 13, wherein the circuit filters a lower-frequency portion of a signal received at the first and second inputs.

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16. (original) The circuit of claim 13, wherein the circuit reduces the distortion of a signal received at the first and second inputs and delivered at the first and second outputs.

17. (original) The circuit of claim 13, further comprising a third output, connected via a second capacitor to the first input, and a fourth output, connected via a third capacitor to the second input.

REMARKS

By this Amendment, no claims are canceled or amended, and no new claims are presented for examination. As a result, claims 1-17 remain pending in the application. The specification is amended to correct inadvertent typographical errors.

Claim Rejections – 35 U.S.C. §112

Pursuant to the above-referenced Office Action, claims 7-8 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

Applicants traverse the rejection and submit that the subject matter of claims 7-8 is fully supported by the specification. As amended herewith, the specification beginning at page 5, line 15 states (with emphasis added):

> Figures 3 and 4, respectively, show POTS splitter designs, using frequency-sensitive inductance devices in accordance with the preferred embodiment, of a central office POTS splitter and a remote end POTS splitter. In these figures, the frequency sensitive device consists of **L3**, **R2**, and **R3**. The low-pass filter is therefore comprised of **L3**, **R2**, **R3**, and **C4** in Figure 3, and **L3**, **R2**, **R3**, and **C3** in Figure 4. Other parts of the circuit will be understood by those of skill in the art as a conventional POTS splitter circuit.
>
> *For purposes of this discussion*, the conventional circuit comprised by **L1** and **C2** in Figure 3, and by **L1** and **C1** in Figure 4, will be referred to as "stage 1" of each of these figures. Similarly, the conventional circuit comprised by **L2**, **C5**, **C6**, and **C3** in Figure 3, and by **L2**, **C5**, **C6**, and **C2** in Figure 4, will be referred to as "stage 2" of each of these figures. Finally, "stage 3" will reference the frequency-sensitive circuit of the preferred embodiment, which comprises **L3**, **R2**, **R3**, and **C4** in Figure 3, and by **L3**, **R2**, **R3**, and **C3** in Figure 4.

It will then be clear that, in Figures 3 and 4, nodes **A** and **B** form the inputs to stage 1, and nodes **C** and **D** are both the outputs of stage 1 and the inputs of stage 2. Nodes **E** and **F** are both the outputs of stage 2 and the inputs of stage 3, and nodes **G** and **H** are the outputs of stage 3.

Accordingly, in the *exemplary* embodiments shown and described in the specification, the frequency-sensitive circuit is depicted as stage 3 having first and second inputs at **E** and **F**, respectively, and first and second outputs at **G** and **H**, respectively. As shown and described, conventional circuits in POTS splitter design are depicted as stage 1 and stage 2. Stage 1 has first and second inputs at **A** and **B**, respectively, and first and second outputs at **C** and **D**, respectively. Stage 2 has first and second inputs at **C** and **D**, respectively, and first and second outputs at **E** and **F**, respectively. However, as clearly stated in the specification beginning at page 7, line 15 (with emphasis added):

> ... In particular, in Figure 3 and Figure 4, the preferred frequency sensitive device that consists of **L3**, **R2**, and **R3**, from stage 3, can be used to replace other conventional transformer/filter circuits, e.g., the **C5**, **C6**, **L2** circuit of stage 2. *This means that a frequency-sensitive circuit as in stage 3 may also appear as the first or second stage.*
>
> Further, the position of the frequency-sensitive inductance device within the POTS splitter will vary the overall performance characteristics of the splitter. *For example, in Figure 4 above, the stage 3 circuit can be switched with the stage 2 circuit, so that their order is reversed,* according to the requirements of the system in which the system is to be installed.

Accordingly, the frequency-sensitive circuit referred to as "stage 3" in the specification may be located anywhere in the POTS splitter design and in any combination with one or both of stage 2 and stage 1 depicted in Figures 3 and 4. As such, there is no set convention for labeling the inputs and the outputs of each stage of the POTS splitter. Applicants are not limited to claiming *only* the exemplary embodiments depicted in Figures 3 and 4. To the contrary, Applicants are entitled to claim the invention in any manner supported by the specification and drawings. In the present case, Applicants have elected in claim 6 to claim a frequency-sensitive electrical circuit reciting the frequency-sensitive inductance device depicted in Figures 3 and 4 between first and second inputs **E** and **F** and first and second outputs **G** and **H** as the "first stage." In claim 7, Applicants have elected to claim the frequency-sensitive electrical circuit of

claim 6 further reciting the conventional transformer/filter circuit depicted in Figures 3 and 4 between first and second inputs **C** and **D** and first and second outputs **E** and **F** as the "second stage." In claim 8, Applicants have elected to claim the frequency-sensitive electrical circuit of claim 6 further reciting the conventional transformer/filter circuit depicted in Figures 3 and 4 between first and second inputs **A** and **B** and first and second outputs **C** and **D** as the "third stage." In other words, Applicants have merely elected to claim the circuits depicted in Figures 3 and 4 by E, F, G, H ("stage 3"); C, D, E, F ("stage 2"); and A, B, C, D ("stage 1") in reverse order. Doing so is fully supported by the disclosure of the specification beginning at page 7, line 15 and reproduced hereinabove. Thus, claims 7 and 8 fully comply with the written description requirement and the rejection is improper. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection to claim 7-8 under 35 U.S.C. §112, first paragraph.

Claim Rejections – 35 U.S.C. §112

Pursuant to the Office Action, claims 7-8 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As discussed above, as depicted in the *exemplary* embodiments shown in Figures 3 and 4, nodes **A** and **B** form the inputs to stage 1, and nodes **C** and **D** are both the outputs of stage 1 and the inputs of stage 2. Nodes **E** and **F** are both the outputs of stage 2 and the inputs of stage 3, and nodes **G** and **H** are the outputs of stage 3. However, the specification beginning at page 7, line 15, further clearly states that the frequency sensitive device from stage 3 can be used to replace other conventional transformer/filter circuits, such as the circuit of stage 2 or stage 1. "*This means that a frequency-sensitive circuit as in stage 3 may also appear as the first or second stage.*" "*For example, in Figure 4 above, the stage 3 circuit can be switched with the stage 2 circuit, so that their order is reversed.*" As claimed in claim 6, stage 3 is the first stage having inputs **E** and **F** and outputs **G** and **H** shown in Figures 3 and 4. As claimed in claim 7, stage 2 is the second stage having inputs **C** and **D** and outputs **E** and **F** shown in Figures 3 and 4. Thus, the outputs of the second stage (**E** and **F**) form the inputs of the claim 6 first stage. As claimed in claim 8, stage 1 is the *second* stage having inputs **A** and **B** and outputs **C** and **D** shown in Figures 3 and 4. Stage 2 shown in Figures 3 and 4

is not claimed. Thus, the outputs of the second stage (**C** and **D**) form the inputs of the claim 6 first stage (**E** and **F**). Accordingly, Applicants respectfully request the Examiner to withdraw the rejection to claims 7-8 under 35 U.S.C. §112, second paragraph.

Claim Rejections – 35 U.S.C. §102

Pursuant to the Office Action, claims 1-6 and 9-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,137,880 (Bella). With regard to independent claims 1, 6 and 13, the Examiner asserts that Bella illustrates in Figure 6 a frequency sensitive electrical circuit **370**, comprising first and second inputs; at least one transformer circuit (**L11**or **L12** or **L13**) having a first winding connected to the first input and a second winding connected to the second input; a first load **374** connected in parallel to the first winding **L12**; a second load **376** connected in parallel to the second winding **L12**; first and second outputs connected to the first and second windings; and a capacitor **C24** connected between the first and second outputs. See Office Action at page 4.

Applicants respectfully traverse the rejection with respect to at least the independent claims 1, 6 and 13. As established by the Declaration Under 37 C.F.R. §1.131 Of Inventor Harley J. Staber filed concurrently herewith (hereinafter "the Declaration"), Applicants completed (i.e., conceived and reduced to practice) the inventions embodied in at least independent claims 1, 6 and 13 in this country or in a NAFTA or WTO member country before the earliest effective filing date of Bella. Declaration at paragraph 6. Specifically, the Record Of Invention attached to the Declaration as Exhibit A shows and describes the same frequency-sensitive inductance device shown in Figures 1-4, described in the specification and claimed in independent claims 1, 6 and 13 of the present application. See Declaration at paragraphs 8-10. Furthermore, the inventions embodied in at least independent claims 1, 6 and 13 were known to work for their intended purposes prior to the earliest effective filing date of Bella. Declaration at paragraph 11. Thus, Bella is not properly available as a prior art reference against the independent claims 1, 6 and 13. For at least the reasons stated above, independent claims 1, 6 and 13 are patentable. Claims 2-5 depend directly or indirectly from patentable base claim 1, and

thus, are likewise allowable for at least the same reasons. Similarly, claims 9-12 and 14-17 depend directly or indirectly from patentable base claims 6 and 13, respectively, and thus, are likewise allowable for at least the same reasons. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claims 1-6 and 9-17 under 35 U.S.C. §102(e).

Claim Rejections – 35 U.S.C. §103

Pursuant to the Office Action, claims 7-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Bella in view of United States Patent 6,567,519 (Ham). See Office Action at page 5.

Applicants respectfully traverse the rejection. As discussed above, the Declaration filed concurrently herewith clearly establishes that Applicants completed (i.e., conceived and reduced to practice) the inventions embodied in at least independent claims 1, 6 and 13 in this country or in a NAFTA or WTO member country before the earliest effective filing date of Bella and before the earliest effective filing date of Ham. Declaration at paragraph 6. Specifically, the Record Of Invention attached to the Declaration as Exhibit A shows and describes the same frequency-sensitive inductance device shown in Figures 1-4, described in the specification and claimed in independent claims 1, 6 and 13 of the present application. See Declaration at paragraphs 8-10. Furthermore, the inventions embodied in at least independent claims 1, 6 and 13 were known to work for their intended purposes prior to the earliest effective filing date of Bella and prior to the earliest effective filing date of Ham. Declaration at paragraph 11. Thus, Bella and Ham are not properly available as prior art references against the independent claims 1, 6 and 13. For at least the reasons stated above, independent claims 1, 6 and 13 are patentable. Claims 7-8 depend directly or indirectly from patentable base claim 6, and thus, are likewise allowable for at least the same reasons. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claims 7-8 under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing remarks, Applicants respectfully request the Examiner to withdraw the rejections to the claims, and to reconsider the application. This Amendment AFTER FINAL is fully responsive to the Office Action and places the application in condition for immediate allowance. In addition, this Amendment AFTER FINAL does not introduce additional claims or new issues that would require further search or consideration. Accordingly, Applicants respectfully request the Examiner to issue a Notice of Allowability for the pending claims. Applicants encourage the Examiner to contact the undersigned directly to further the prosecution of any remaining issues, and thereby expedite allowance of the application.

This Amendment AFTER FINAL does not result in any more independent or total claims than paid for previously. Accordingly, **no fee for excess claims is believed to be due.** The Examiner is hereby authorized to charge any other fee due in connection with the filing of this response, including any excess claims fee, to Deposit Account No. 19-2167. If a fee is required for an extension of time under 37 C.F.R. §1.136 not already accounted for, such an extension is requested and the fee should likewise be charged to Deposit Account No. 19-2167. Any overpayment should be credited to Deposit Account No. 19-2167.

Respectfully submitted,

Christopher C. Dremann
Attorney for Applicants
Registration No. 36,504
P. O. Box 489
Hickory, N. C. 28603
Telephone: 828/901-5904
Facsimile: 828/901-5206

Dated: July 14, 2004